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BOOLEAN CHAOS

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Abstract:

The article discusses the deterministic chaos that occurs in a simple digital circuit consisting of logic gates that are not synchronized by an external signal. The pulses at the output of the circuit have an ultra-wideband spectrum in the range from DC to 2 GHz or more. The behavior of the circuit is qualitatively described using a Boolean model, which is updated autonomously. The signal transit time in the model depends on the set of previous states of the elements. The model filters short pulses, the presence of which has been confirmed experimentally. Chaos in digital circuits can be used as a source of ultra-wideband radio signals.

Keywords: Digital circuit, exponential sensitivity, Boolean circuits, topology, chaos.

With a very simple digital circuit, deterministic chaos can be obtained, which is characterized by a broadband spectrum and rapid divergence of adjacent trajectories. We will call this behavior of the circuit "Boolean chaos" and show that it can be described by a model in which the state update time is determined by the signal propagation time. Our circuit can be used in secure broadband systems, to create an economical sensor or beacon, or as a basis for building a high-speed random number generator. It can also be used to study the fundamental aspects of the behavior of complex circuits.

The proposed circuit consists of three nodes implemented on high-speed general-purpose logic gates. The voltage sampling at any point in the circuit has a non-repeating structure with pronounced logical transitions. It exhibits exponential sensitivity to initial conditions and has a wide spectrum from DC to 2 GHz or more. Since the circuit contains feedback loops with incommensurable delays, it spontaneously enters dynamic states in which the pulses have the smallest possible width. In this mode, minor changes to the delay create havoc. We assume that this behavior will be typical for a wide class of systems described using stand-alone Boolean chains.

Boolean strings have been studied in a variety of contexts. For systems that exhibit switching behavior, such as logic diagrams or gene distribution diagrams, it is often useful to assume that system variables only take two values (for example, "high" and "low"), which are updated by boolean functions. Deterministic logic models often include an external process, such as a clock that synchronizes all updates, or another device that determines the order of updates for each item. The state space of such models is discrete and finite. Thus, they can only have periodic attractors. On the other hand, in many physical or biological systems, information propagates between logical elements with delays that can be different for each connection. To predict the behavior of such systems, it is necessary to accurately determine the moments in time at which state changes occurred, which makes the state space continuous. The mathematical description of these autonomous Boolean systems has been much less studied, although it is known that they are capable of exhibiting an aperiodic sample structure if the gates have an instantaneous response.

Gil et al presented logic delay equations (BDE) for studying ideal gate logic gates. The dynamics of state changes (here called "events") in circuits is studied under the assumption that the gates can process the incoming signal as quickly as necessary. The behavior of the system as a whole becomes more complicated when the number of events per unit of time changes according to a power law. This behavior is assumed to be common for a wide class of Boolean strings.

The complex behavior of the system, described in, leads to an ultraviolet catastrophe (paradox of thermodynamics), which cannot be reproduced experimentally, since the existing logic gates are not capable of processing arbitrarily short pulses. We have found that complex behavior of this kind turns into deterministic chaos in our experimental systems and in numerical simulations if we take into account the disadvantages, as described below. Taking into account the complex behavior of a wide class of ideal BDEs, as well as our observations of deterministic

chaos in a simple experiment with a three-node circuit, we assume that a wide class of experimental Boolean circuits will exhibit chaos.

The topology of our stand-alone logic circuit is shown in Figure 1 (a). It consists of three nodes, each with two inputs and one output connected to two other inputs. Let τji (i, j = 1,2,3) denote the time required for the signal to propagate from node i to node j. Nodes 1 and 2 perform an exclusive OR (XOR) operation, and node 3 performs the same inverse operation (XNOR) as shown in the truth table in Figure 1 (a). The considered circuit is in an unstable state (does not have a stable fixed point), which leads to oscillations. The total signal delay is determined by the internal delay of each gate (XOR or XNOR) and the external delay in connecting wires, inverters or Schmitt triggers. It should be emphasized that there are no clock pulses in the system, i.e. the signal processing speed is determined by the delay of the logic gates

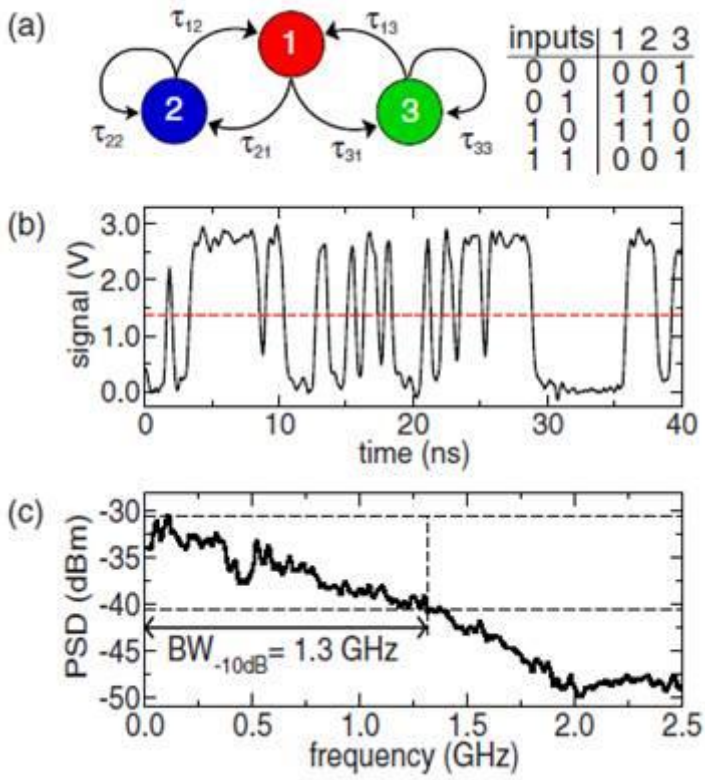

Fig. 1.

(a) Boolean chain topology with chaos and truth table for logical operations performed by nodes 1, 2 (XOR), and 3 (XNOR);

(b) time base of the signal;

(c) Power spectral density (PSD) for VCC = 2.75V.

The dynamics of our circuit was observed using a high-impedance active probe and a digital oscilloscope with a bandwidth of 8 GHz and a sampling rate of 40 GS / s. Figure 1 (b) shows the typical behavior of the circuit at the output of node 2. The time sweep of the signal has a complex and non-repetitive structure with well-defined high and low values that indicate the logical behavior of the circuit. The voltage rise time is about 0.2 ns (which is close to the limit for logic gates used in the circuit). The minimum, average and maximum pulse durations in a chaotic sequence are 0.2, 2.4, and 12 ns, respectively. The spectrum of pulses (Fig. 1c) lies in the frequency band from zero (direct current) to ~ 1.3 GHz (at a level of -10 dB). The frequency response is relatively flat until 400 MHz and then decays inversely with frequency.

We found that the dynamics of the circuit depends on the supply voltage VCC of the logic elements, which is further considered as a bifurcation parameter. This dependence of dynamics on VCC can be explained by the fact that all the timing characteristics of the gates, such as transient delay, rise and fall times, etc., are non-linear with VCC. The bifurcation diagram of the circuit (Fig. 2) is built for a time interval of 1 μs, at which the output voltage V (t) of node 2 is converted into a Boolean variable x (t) for a given VCC as follows. Let us set the threshold voltage VCC / 2, if V (t) <VCC / 2, then x (t) = 0, if V (t) ≥VCC / 2, then x (t) = 1, as shown by the dashed line in Fig. 1 (b).

Thus, we get a sequence of logical values x (t), which is then analyzed to determine the time between adjacent transitions from "low" to "high". These time intervals are plotted on the bifurcation diagram for each VCC value in the range of 0.9 V to 3.3 V in 5 mV steps.

The bifurcation diagram (Fig. 2) shows areas of complex behavior, where the points practically merge into one wide band. The intervals in which this does not occur correspond to the areas of periodic behavior. The presence of several distinct periodic bands indicates that the circuit is not overly sensitive to small changes in VCC. Moreover,

its complex behavior manifests itself over a wide range of supply voltages, especially at VCC> 2.40 V when the logic gates are operating at maximum speed.

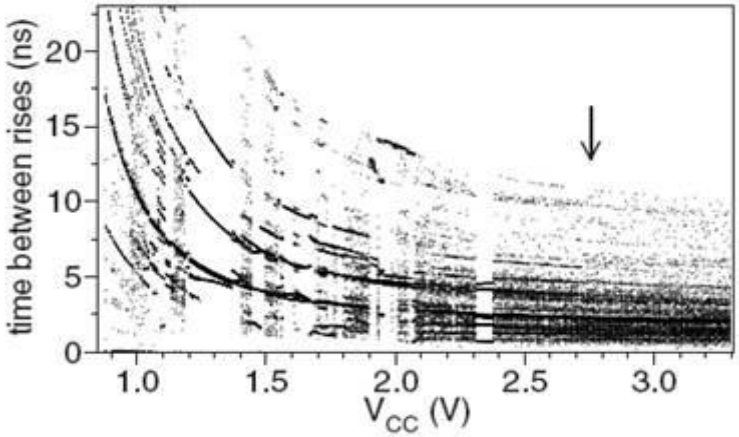

Fig. 2. Bifurcation diagram of a Boolean chain. The arrow indicates the VCC value at which complex behavior is observed, as shown in Fig. 1 (b).

The exponential divergence of trajectories with approximately the same initial conditions is a sign of chaos. This discrepancy is indicated by the positive Lyapunov exponent. To estimate the largest Lyapunov exponent, the following method is proposed. We will measure the voltage over a long period of time and then convert it to a sequence of binary variables x (t). For two arbitrary segments of the sequence x (t) starting at times ta and tb, we define the Boolean distance d (s) between them as a function of time s [11]

$$d(s) = \frac{1}{T}\int_{s}^{s+T} x(t' + t_a) \oplus x(t' + t_b)dt', \qquad (1)$$

where T = 10 ns - fixed parameter and XOR operation. On each interval T for which d (0) <0.01 (ln d (0) <−4.6), we find all pairs ta and tb in the sequence x (t). Typically, a 40 μs sequence contains about 3000 such pairs. We then calculate <ln d (s)>, where "<>" means the average over all matching pairs (ta, tb).
Figure 3 (a) shows two typical voltage patterns V (s + ta) and V (s + tb), and Figure 3 (b) shows the corresponding boolean variables x (s + ta) and x (s + tb). When you zoom in, you can see a slight out of sync between the two pulse trains. At the selected scale, this is clearly visible after 20 ns, and after 30 ns, the sequences become independent.

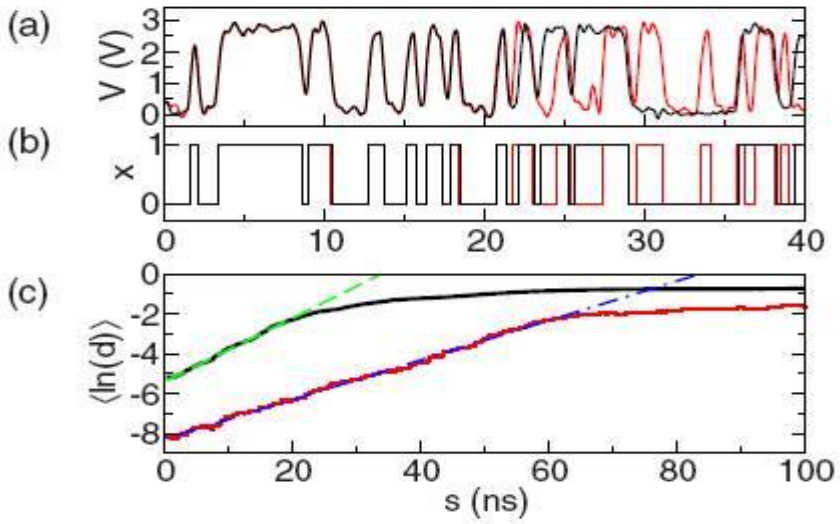

Fig. 3.
(a) Typical samples of similar voltages for VCC = 2.75V;
(b) Boolean variables corresponding to the stresses in Figure 3 (a);
(c) Logarithm of Boolean distance as a function of time, averaged over the attractor of the state space of the chain for experimental data (upper curve) and simulations (lower curve).

To assess the observed results at a qualitative level, let us determine the largest Lyapunov exponent for the attractor. The upper curve in Fig. 3 (c) has an almost constant slope (dashed line) for s <20 ns and approaches the maximum value ln 0.5 ≈ −0.69, for which x (s + T + ta) and x (s + T + tb) are independent. We will assume that in the region of constant slope the divergence of initially identical segments is exponential, i.e. ln d (s) = ln d0 + λabs, where λab is the local Lyapunov exponent. Averaging λab over all pairs of identical segments is an estimate for the largest Lyapunov exponent λ of the system. When looking for a neighboring element in a sequence, as described in [13], we used logical distance instead of delay coordinates and found that λ = 0.16 ns - 1 (± 0.02 ns - 1) indicates chaos in the circuit.

To test our method, we switched the system to an almost periodic mode (VCC = 2.35V) and repeated the analysis. As a result, the logical distance, as expected, remained small (<ln d> <−4). Moreover, it was found that our signal was not caused by a hypothetical linear increase in the correlated noise. This conclusion was made on the basis of a comparison of experimental data with a fictitious signal obtained by rearranging the members of the sequence while maintaining its power spectrum and probability distribution. For a better understanding of the observed results, consider the Boolean delay equations

$$x_1(t) = x_2(t - \tau_{12}) \oplus x_3(t - \tau_{13}),$$

$$x_2(t) = x_1(t - \tau_{21}) \oplus x_2(t - \tau_{22}),$$

$$x_3(t) = x_1(t - \tau_{31}) \oplus x_3(t - \tau_{33}) \oplus 1, \qquad (2)$$

where xi is the logical state of the i-th node, and "1" inverts the variable (NOT). The values of τji are given in the bottom row of Table I. Using the initial conditions x1 (t) = x2 (t) = x3 (t) = 0 for t <0, one can see that the average rate of events for x1 (t) (or any other variable) grows according to a power law with exponent ~ 2, which indicates a complex behavior of the chain, as established by Gil and Mullhaupt.

Таблица I

ji	12	13	21	22	31	33
τ^r_{ji} (ns)	3.13	4.30	3.20	2.47	3.08	3.62
τ^f_{ji} (ns)	2.92	4.09	2.97	2.27	2.85	3.42

Such an increase in the frequency of events is impossible in an experimental system, since real logical elements cannot instantly change their state. We found that the main reason for non-ideal network behavior is the delay of elements that form a connecting arc between the XOR and XNOR nodes. The latency in these nodes themselves has much less effect on the behavior of the circuit. To qualitatively assess the imperfect behavior of each of the connecting arcs, we measured the propagation delay of the signal through it. Based on the data obtained, three types of non-ideal behavior can be distinguished:

1) Suppression of short pulses or filtering, which does not allow pulses with a duration less than or equal to the minimum, to pass through the logic element ;

2) asymmetry of logical states, due to which the signal propagation delay through a logical element depends on how its logical state changes from "low" to "high" or vice versa;

3) The degradation effect, which leads to a change in the propagation delay of events when they quickly go one after another.

Note that these types of non-ideal behavior have been proposed for Boolean idealizations of electrical and biological circuits. This suggests that the study of these effects can have a wide range of applications.

In our model, the listed types of imperfect behavior are taken into account as follows. First, to describe the degradation effect of signal propagation along an arc, we introduce a new variable, as was done in [14]. ... Let tn be the time at which event n occurs at the beginning of the arc, and t`n be the time at which the corresponding event is observed at the end of the arc. Note that tn is not related to arc degradation, but t`n is related.

$$P_n \equiv t_n + \tau^k_{ji} - t`_{n-1}, \qquad (3)$$

τ^k_{ji} - where τkji is the nominal arc delay for rise (k = r) or fall (k = f) events. Typical behavior of the propagation delay τf33, $n \equiv t_n - t`_n$ for decay events depending on P_n for arc 3-3 is shown in Fig. 4. The experimental data for each arc were interpolated by the formula

$$\tau^k_{ji,n} = \tau^k_{ji} + Ae^{-BPn} \cos(\Omega P_n + \varphi), \qquad (4)$$

где τ^k_{ji}, A, B, Ω, и φ – adjustable parameters, and $\tau^k_{ji,}$, n is the propagation delay of the nth event along the arc ji. The minimum interval Pmin is determined from the data as the shortest time interval during which the event is observed. The only parameter that strongly depends on the particular arc and the sign of the event is τkji (see Table I). Based on the data interpolation shown in Fig. 4, we found the following parameter values: A = 1.28 ns, B = 1.4 ns − 1, Ω = 4.8 rad / s, φ = 0.062 rad, and Pmin = 0.48 ns, which we are going to use for all arcs in the circuit. The next stage of our simulation is the solution of the Boolean delay equations (2) with the replacement of $\tau^k_{ji,}$ by the corresponding $\tau^k_{ji,}$. For each event, we estimate Pn, if Pn <Pmin, the current and previous events are discarded. Otherwise, we adjust the new transition time value with (4).

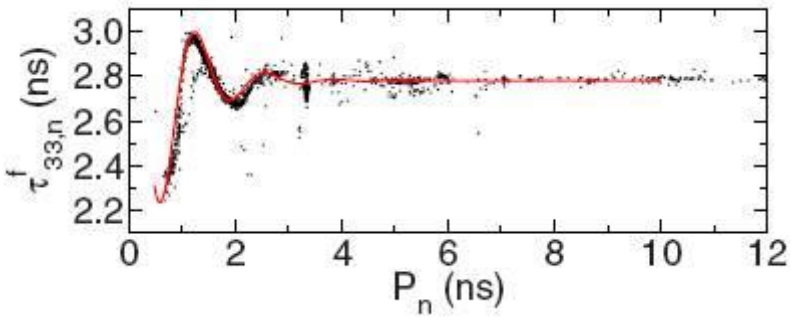

Fig. 4. Measured during the experiment the transient delay of the event along the arc 3-3 (points) as a function of Pn. The pulses are subject to degradation effects. Interpolation of measured values (continuous line), discussed in the text.

Using the sequences obtained in the simulation, we calculate <ln d> [Fig. 3 (c)] for the initial value of the logical distance d (0) <0.001 [ln d (0) <-6.9] for which pairs are selected. The obtained value λ = 0.10 ns - 1 (± 0.02 ns - 1) indicates that the modified model, which takes into account the imperfect behavior of logic elements, demonstrates deterministic chaos. In addition, the values of the Lyapunov exponent obtained experimentally and by means of simulation are very close; therefore, the model takes into account the main properties of our electronic circuit.

A detailed study of each specific type of non-ideal behavior is beyond the scope of this work.

Thus, we found that the sequence of changes in the states of an autonomous logical chain demonstrates deterministic chaos. This behavior is very different from what is observed in periodically updated (synchronized) logical networks, for which only periodic behavior is predicted. Our research can be important in understanding other naturally occurring circuits. For example, chaos was found in systems of differential equations describing gene distribution chains, although the source of the chaos was not found. To pass to other natural systems, it is necessary to measure the parameters of imperfect logical elements. We assume that the three observed effects ,,, are the main ones, although they are difficult to investigate directly. Further theoretical research is also needed to determine the limits of applicability of the modified Boolean delay equations to the design and understanding of the behavior of real circuits.

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